CLAIMS

What is claimed is:

1. A computer system comprising:

a bus; and

a chipset, coupled to the bus, to detect the slew rate of a signal transmitted over the bus via the chipset, and to adjust the slew rate based upon the state of the signal.

2. The computer system of claim 1 wherein the chipset comprises:

a slew rate detection mechanism to detect the slew rate and generate a signal to indicate the status of the slew rate; and

control logic, coupled to the slew rate detection mechanism, to receive the signal and modify the slew rate based upon the signal.

3. The computer system of claim 1 wherein the chipset further comprises an input/output (I/O) buffer coupled to the control logic.

4. The computer system of claim 2 wherein the control logic reduces the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too fast.

5. The computer system of claim 2 wherein the control logic increases the slew rate if the signal received from the slew rate detection mechanism indicates

that the slew rate is too slow.

6. The computer system of claim 2 wherein the slew rate detection mechanism includes a capacitor, coupled to the bus, to integrate the received signal current.

7. The computer system of claim 6 wherein the slew rate detection mechanism further includes:

a reference current generator to generate a reference current; and

a comparator to compare the received signal current to the reference current.

8. The computer system of claim 7 wherein the slew rate detection mechanism further includes:

a first converter, coupled to the capacitor and the comparator to convert the signal current to a signal voltage; and

a second converter, coupled to the reference current generator and the comparator to convert the reference to a reference voltage.

9. The computer system of claim 6 wherein the comparator is an operational amplifier.

10. The computer system of claim 1 wherein the bus is a high-speed bus.

11. A computer system comprising:

a main memory device;

a memory bus coupled to the main memory device; and

a memory controller, coupled to the bus, to detect the slew rate of a signal transmitted over the bus via the chipset, and to adjust the slew rate based upon the state of the signal.

12. The computer system of claim 11 wherein the memory controller comprises:

a slew rate detection mechanism to detect the slew rate and generate a signal to indicate the status of the slew rate; and

control logic, coupled to the slew rate detection mechanism, to receive the signal and modify the slew rate based upon the signal.

13. The computer system of claim 12 wherein the control logic reduces the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too fast.

14. The computer system of claim 12 wherein the control logic increases the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too slow.

15. The computer system of claim 12 wherein the slew rate detection mechanism includes a capacitor, coupled to the bus, to integrate the received signal current.

16. The computer system of claim 15 wherein the slew rate detection mechanism further includes:

a reference current generator to generate a reference current; and

a comparator to compare the received signal current to the reference current.

17. The computer system of claim 16 wherein the slew rate detection mechanism further includes:

a first converter, coupled to the capacitor and the comparator to convert the signal current to a signal voltage; and

a second converter, coupled to the reference current generator and the comparator to convert the reference to a reference voltage.

18. A method comprising:

transmitting a signal from an input/output (I/O) buffer within a chipset over a bus;

receiving the signal at a slew rate detection mechanism within the chipset via the bus;

generating a signal indicating the status of the slew rate; and

adjusting the slew rate at control logic within the chipset based upon the signal.

19. The method of claim 18 further comprising generating a reference current at the chipset.

20. The method of claim 19 further comprising:

converting the signal current to a signal voltage;

converting the reference current to a reference voltage; and

comparing the reference voltage to the signal voltage.

21. The method of claim 18 wherein adjusting the slew rate comprises modifying the amplification of a second signal at the I/O buffer.

22. An apparatus comprising:

a slew rate detection mechanism to detect the slew rate of a signal transmitted over a bus via the memory controller, and to adjust the slew rate based upon the state of the signal; and

detect the slew rate and generate a signal to indicate the status of the slew rate bus

23. The apparatus of claim 22 wherein the slew rate detection mechanism generates a signal to indicate the status of the slew rate bus

24. The apparatus of claim 23 further comprising control logic, coupled to the slew rate detection mechanism, to receive the signal and modify the slew rate based upon the signal.

25. The apparatus of claim 24 further comprising an input/output (I/O) buffer coupled to the control logic.

26. The apparatus of claim 22 wherein the slew rate detection mechanism includes a capacitor, coupled to the bus, to integrate the received signal current.

27. The apparatus of claim 26 wherein the slew rate detection mechanism further includes:

a reference current generator to generate a reference current; and

a comparator to compare the received signal current to the reference current.

28. The apparatus of claim 27 wherein the slew rate detection mechanism further includes:

a first converter, coupled to the capacitor and the comparator to convert the signal current to a signal voltage; and

a second converter, coupled to the reference current generator and the comparator to convert the reference to a reference voltage.